Use of metal–oxide–semiconductor capacitors to detect interactions of Hf and Zr gate electrodes with SiO_2 and ZrO_2

Hf + Zr Metal gates Unstable on ZrO_2 MOCVD for ZrO_2

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Metal–oxide–semiconductor capacitors were used to study the interaction of Hf and Zr gate electrodes on SiO_2, $ZrSi_xO_y$, and ZrO_2. A large reduction in the SiO_2 equivalent oxide thickness accompanied by an increase in the leakage current was observed with Hf and Zr electrodes when subjected to anneal temperatures as low as 400 °C. The reduction in electrical thickness as observed from the capacitance–voltage measurements was attributed to the combination of (a) physical thinning of the SiO_2 and (b) formation of a high-K layer. A severe instability of Zr and Hf electrodes was also observed on $ZrSi_xO_y$ and ZrO_2 dielectrics. This behavior of Zr and Hf gates was attributed to high negative enthalpy of oxide formation and high oxygen solubility resulting in the reduction of the gate dielectric and subsequent oxygen diffusion to the gate electrode. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1380240]

As silicon complementary metal–oxide–semiconductor devices (MOS) are scaled below 100 nm, advanced high-K gate dielectrics will be required to obtain oxide equivalent thickness $T_{ox\text{-}eq}$, <1.0 nm. As $T_{ox\text{-}eq}$ decreases, the capacitance associated with the depletion layer at the polycrystalline-Si-gate dielectric interface becomes increasingly important, making it necessary to consider alternative gate electrodes, such as metals.[1,2] The search for metallic gates faces many challenges since they must have appropriate work functions and be stable with the gate dielectric during subsequent high-temperature processing steps. To replace n^+ and p^+ polycrystalline silicon and maintain scaled performance, it is necessary to identify pairs of metals with work functions that are, respectively, within 0.2 eV of the conduction- and valence-band edges of Si, i.e., the work function ϕ_m, for N- and P-channel gates must be near 4 and 5 eV, respectively.[3]

In this work, we have investigated the properties of hafnium and zirconium gate electrodes on SiO_2 and high-K dielectrics. The motivation behind selecting these gates is based on their low-work-function values appropriate for NMOS devices. It has been reported that both Zr and Hf have work-function values near 4.0 eV.[4] Moreover, no prior reports on the electrical properties of Hf and Zr metals as gate electrodes exist on either SiO_2 or emerging high-K dielectrics. Since emerging high-K dielectrics include ZrO_2, HfO_2, or $ZrSiO_4$, it is very timely to evaluate the properties of Zr and Hf gates on these dielectrics.

Field oxide isolated overlap capacitors were fabricated on n- and p-type wafers using lift-off to define the gate electrodes. Thermal oxide controls of varying thicknesses were grown at 900 °C. ZrO_2 and Zr-silicate dielectrics were formed using metal–organic chemical-vapor deposition of $C_{16}H_{36}O_4Zr$. An *in situ* sputtered tungsten capping layer was deposited following the Hf and Zr deposition to ensure contact to the underlying layer and to avoid oxidation of Hf and Zr electrodes. The base pressure of the chamber in which the metal films were deposited was $<2\times10^{-8}$ Torr. Following gate definition, the samples were annealed in 10%H_2/N_2 at 400 °C for 30 min. An HP4284A was used to measure the capacitance–voltage characteristics. The capacitor area of the devices measured was 2.5×10^{-5} cm^2. The flatband V_{FB} voltage and equivalent oxide thickness for the capacitors were extracted from $C-V$ curves using NCSU $C-V$ analysis program.[5]

Figure 1 shows the capacitance versus voltage curves for SiO_2 dielectrics with Hf gates for various anneal conditions. The as-deposited condition retains some sputtering damage and, therefore, results in a V_{FB} shift from the expected V_{FB}. The capacitance value of the as-deposited case resulted in a T_{ox} that matched the physical thickness of the grown SiO_2. After a 400 °C anneal, the V_{FB} shifted to the appropriate[7] value for Hf gates indicating that the sputtering damage was removed. However, the accumulation capacitance value dramatically increased, indicating that T_{ox} was considerably thinner than the as-grown thickness. Anneals done at 500 °C

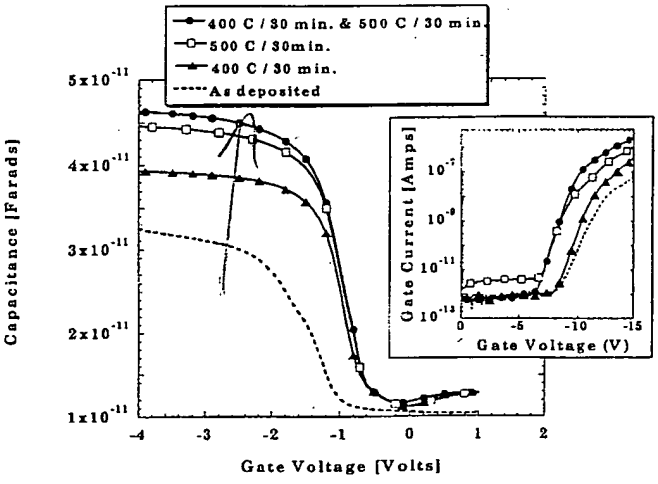

FIG. 1. Capacitance–voltage change of SiO_2 dielectrics with hafnium electrodes subjected to various annealing conditions. The inset shows the corresponding gate current changes.

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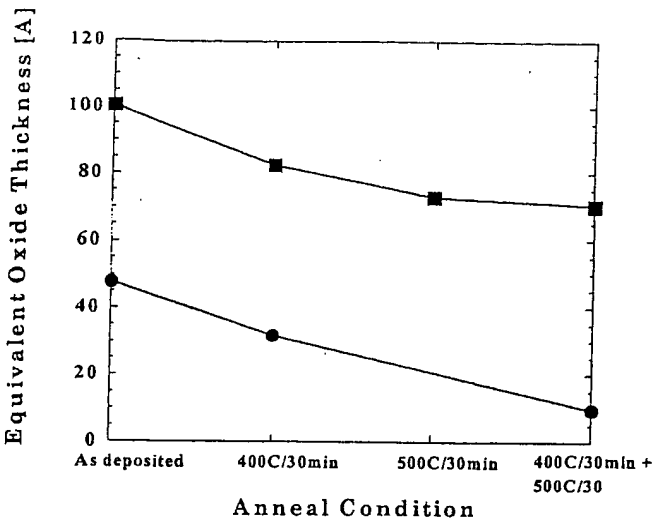

FIG. 2. Quantification of the oxide thickness reduction with Hf gates as a function of various starting thicknesses and anneal temperatures.

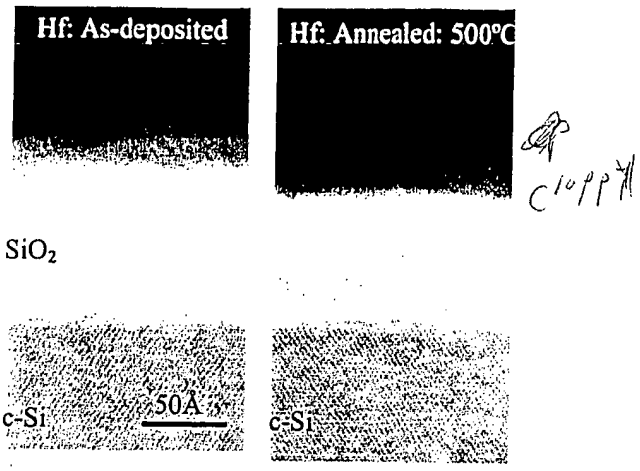

FIG. 3. Cross-sectional transmission electron micrograph of Hf gates on SiO_2 for as-deposited and after a 500 °C anneal. The TEM indicates the physical reduction of the SiO_2 layer after the anneal, which agrees with the electrical data.

further increased the capacitance without affecting the V_{FB} values. A cumulative anneal of 400+500 °C resulted in even larger increases of accumulation capacitance values. The inset of Fig. 1 displays the gate leakage current as a function of the gate voltage of the same samples. As shown, the leakage current increases indicating that as the capacitance increases, the leakage current through the gate dielectric also increases. In order to verify whether the changes in leakage current are coming entirely from the physical thickness reduction of the SiO_2, Fowler–Nordheim tunneling current modeling assuming a typical effective mass of $0.42m_0$ was performed. A barrier height of 3.2 eV was chosen based on the work-function values ($\phi_m \sim 4$ eV) obtained from our capacitance–voltage curves, which also agrees with the bulk work-function values published in the literature for hafnium. If the oxide thickness as obtained from the $C-V$ curve was used, the modeled leakage current was significantly higher than the experimental data, indicating that the physical thickness of the stack is larger than the electrical thickness value obtained from $C-V$. This indicates that the reduction in SiO_2 is being accompanied by the formation of a high-K layer. To understand this, cross-sectional transmission electron microscopy (TEM) was performed on unannealed and annealed (500 °C) Hf gates and the results are shown in Fig. 2. As shown, that along with a physical thinning of the SiO_2 layer after a 500 °C anneal, there is also the presence of an amorphous layer between the Hf and the SiO_2 regions. If the physical oxide TEM thickness (obtained by adding both the light and dark regions) is used in the current–voltage modeling, then a much more reasonable fit is obtained to the measured data, although accurate analysis would involve knowledge of effective mass within the top layer and all the band offsets. An average barrier height, obtained by extracting the slope of J/E_{ox}^2 vs $1/E_{ox}$ curves, resulted in a barrier height value of 2.9 eV, close to the 3.2 eV value assumed earlier. The use of this barrier height with the physical thickness obtained from TEM results in an excellent fit to the experimental data, thereby verifying the presence of a high-K layer.

In order to obtain compositional information of the interface layer between the Hf and the SiO_2, x-ray photoelectron spectrometry (XPS) depth profiling was performed. Near the gate electrode and dielectric interface, we obtained a mixture of signals including primarily Hf–O bonds with some Hf–Si bonding. The inherent limitation of XPS analysis prevented the accurate identification of this layer, however, the above leakage current analysis suggests the presence of a high-K dielectric.

The capacitance increase effect on SiO_2 with the Hf gate electrode as a function of various starting thicknesses is quantified in Fig. 3. As shown, a starting thickness of 50 Å was reduced to ~10 Å even under a very moderate temperature anneal of 400+500 °C/30 min. The same phenomenon was also observed with Zr gates that were subjected to similar temperature anneals.

To understand the mechanisms behind the reduction of SiO_2 at such low temperatures (400–500 °C), it is insightful to investigate the role of oxygen solubility of these metals. It has been reported that metals such as Zr, Hf, Ti, and V have very high oxygen solubility and high negative free energy of formation of oxide and can easily reduce SiO_2 at temperatures higher than 650 °C. In fact, it has been reported that when these metals are placed on SiO_2 and annealed above a critical temperature, they result in the formation of a monosilicide adjacent to the SiO_2 and metal oxide on top.[6] This is attributed to the reduction of SiO_2 in the presence of the metal atoms. The released oxygen then diffuses from the dielectric–metal interface upward to the metal electrode and accumulates within the metal due to its high oxygen solubility. The excess Si left near the electrode–dielectric interface reacts with the metal atoms to form a silicide region. This reaction continues until the metal region on top is completely converted to a metal oxide. In our work, we have found that the reduction of SiO_2 is occurring at temperatures *as low as 400°C*, significantly lower than reported earlier. One possible reason why earlier work did not detect any reaction at such low temperatures may be related to the use of Rutherford backscattering (RBS) to detect reaction layers and the use of very thick SiO_2 films. RBS does not have the resolution to detect reaction layers that are <150 Å. Since capacitance is

sensitive to changes in thickness on the order of angstroms, the use of MOS capacitors provides a very sensitive tool to measure changes in the dielectric at the gate electrode/dielectric interface. A change in either V_{FB} or C_{ox} would indicate a reaction layer at the gate electrode–dielectric interface. The use of these high-sensitivity MOS capacitors has allowed us to detect reactions between SiO_2 and Hf and Zr gates occurring at temperatures as low as 400 °C. The RBS analysis in Ref. 6 indicated that the interfacial layer formed at the Zr/SiO_2 interface was primarily a monosilicide. However, RBS is known for its poor oxygen sensitivity and may not accurately reflect the composition of this layer. As discussed earlier, our XPS analysis of the interfacial region revealed the presence of oxygen in the form of Hf–O bonds. Furthermore, current–voltage analysis also supported the presence of a high-K dielectric layer between the Hf and SiO_2. A complete chemical analysis of the interface layers would require more sensitive techniques such as electron-energy-loss spectroscopy.

In order to evaluate the above metal gates on high-K dielectrics, Hf and Zr gates were also evaluated on ZrO_2 and $ZrSi_xO_y$ MOS capacitors. In this case, the gate stacks completely degraded after a forming gas anneal and resulted in *unrealistically high capacitance* values. The leakage of these high-K gate-stack films was extremely high following the anneal. The explanation of the instability of Hf and Zr on ZrO_2 dielectrics can also be explained by high oxygen solubility of these metals. When these metals are in contact with dielectrics such as ZrO_2, the oxygen from the dielectrics can easily spread out in the metal forming a metal–oxygen solid solution. This effect has, in fact, been observed when Ti is placed in TiO_2, Zr on ZrO_2, and Ta on Ta_2O_5.[6,7] It should be noted that if the anneal temperatures are low then the oxygen can only redistribute and dissolve but not chemically react.

In summary, we have evaluated Zr and Hf gate electrodes on SiO_2 and high-K dielectrics annealed under modest temperatures. MOS capacitor results indicated drastic instabilities of both Hf and Zr gates on all dielectrics studied. The decrease in electrical thickness was attributed to a combination of both SiO_2 reduction and high-K layer formation. This was attributed to the high oxygen solubility of these metals, which can reduce the dielectrics underneath and scavenge their oxygen. These metals have very high negative enthalpy of formation, which indicates their ease of oxidation. Therefore, gate metals such as Zr, Hf, Ti, V, etc., will display severe instabilities on the dielectrics such as SiO_2, Zr, and Hf oxides and silicates and are, therefore, unsuitable.

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